X-711-71-500

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10^5 PULSE HEIGHT ANALYZER FOR USE IN HIGH ENERGY COSMIC RAY EXPERIMENTS (HECRE) ON HIGH ALTITUDE BALLOON FLIGHTS

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GSFC — GODDARD SPACE FLIGHT CENTER —
GREENBELT, MARYLAND

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INTRODUCTION

This report describes a wide dynamic range pulse height analyzer system developed for use on High Energy Cosmic Ray Experiment (HECRE) Balloon Flights. A wide dynamic range of 10^5 is obtained by extending the range of a basic 1024 channel analyzer through the use of multiple ranges and range selection. The system described here contains four 10^5 pulse height analyzers. Each 10^5 pulse height analyzer consists of a group of cordwood welded modules mounted and interconnected on a printed circuit card. Four of these card assemblies, the required clock drive circuitry (discrete components mounted and interconnected on a separate card) and three input-output connectors are interconnected and mounted on the system board, as shown in Figure 1.

SYSTEM OPERATION

Reference (a) describes the general operation of a wide range pulse height analyzer which makes use of multiple ranges and range selection. The system developed for the HECRE Balloon Flights makes use of a basic 1024 channel analyzer and 4 separate ranges of X1, X1/5, X1/25 and X1/125. Figure 2 is a block diagram of this 10^5 pulse height analyzer. The four inputs (from the detector pre-amplifiers) feed identical delay and linear gate chains. The delay is provided to allow the instrumentation logic system (not described in this report) sufficient time to determine whether or not an event should be processed (pulse height analyzed) and the appropriate linear gate opened. The outputs of the four linear gates are connected in parallel and feed a single sweep. Essentially, the sweep converts the input pulse from the opened linear gate to an output pulse with a width proportional to the input pulse amplitude. This output pulse drives the P.H.A. (pulse height analyzer) output gate which then allows the pulses from a free running 500 kHz square wave oscillator to pass through to the output. Thus, the output pulse train will contain a total number of pulses proportional to the input pulse amplitude. As indicated in Figure 2, an enable pulse initiates the sweep and output pulse train. The enable pulse is of relatively short duration and is generated by the clock drive circuitry when the instrumentation logic indicates an event to be processed. This arrangement assures that the output pulse train always starts at the trailing edge of an oscillator pulse (eliminating jitter error) and that noise is very unlikely to generate spurious output pulse trains. It will be noted that the X1, X1/5 and X1/25 inputs from the detector

also drive top of range threshold detectors. The outputs from these threshold detectors feed the four range decision circuit. Also driving the four range decision circuit are a sequence of clock pulses. These are the reset, write and transfer clock pulses. These clock pulses are also generated by the clock drive circuitry when the instrumentation logic system indicates an event to be processed. The outputs of the four range decision circuit drive their associated linear gates. Thus, dependent on the range of the input signal, the appropriate top of range threshold detectors are actuated and through the four range decision circuit, the correct linear gate, X1, X1/5, X1/25 or X1/125 is opened. Bistables in the four range decision circuit generate the bits S1 and S2 which indicate which linear gate is opened and what multiplying factor is to be applied to the output pulse train count.

The linear range of input signals at all four inputs to the 10^5 pulse height analyzer is 2.5 millivolts to 2.0 volts with the input limited at 2.5 volts to prevent overdrive. The output pulse train yields one output pulse per 2.5 millivolts at the input. The thresholds of the X1, X1/5 and X1/25 top of range threshold detectors are all set at 2.0 volts. Table 1 summarizes the characteristics of the 10^5 pulse height analyzer.

10^5 PULSE HEIGHT ANALYZER INTERCONNECT

Figure 3 is an electrical interconnect diagram of one of the 10^5 pulse height analyzer assemblies. This shows the connections between the cordwood welded modules (shown as closed rectangles with terminals), delay lines, discrete components and input-output terminals. The X1, X1/5, X1/25 and X1/125 input signals from the detector come into terminals 14, 16, 20 and 18, respectively, and drive delay lines. The resistors in the input and output circuits of the delay lines (for example, R1 and R2 for delay line "A") are selected to match the impedance of the delay line. The inductors between pin 11 and common of the linear gates (for example, L1 for linear gate "A") are selected to set the linear gate open time. In this system the inductance used with all four linear gates was 3300 microhenrys which yields a linear gate open time of approximately 6.0 microseconds. The capacitors connected across these inductors (C5 through C8) are selected to eliminate spurious linear gate outputs when the linear gates are opened. The X1, X1/5 and X1/25 input signals also drive their respective top of range threshold detectors through attenuators (for example, R9-R10 for the X1 input signal). The three top of range threshold detectors are contained in a single module. The T.B.D. resistors in the attenuators are selected so that the input signal at the top of range threshold is 2.0 volts. Inductors L5, L6 and L7 are selected to yield output pulses of approximately 6.0 microseconds at or above the top of range threshold. The value of inductance for L5, L6 and L7 is 3300 microhenrys.

Table 1

10^5 Pulse Height Analyzer Characteristics

	Range I	Range II	Range III	Range IV
Input to Detector (channel)	1-800	800-4000	4000-20,000	20,000-100,000
Detector X1 Input (mv.)	2.5-2000	Limited 2.5v	Limited 2.5v	Limited 2.5v
Detector X1/5 Input (mv.)	0.5-400	400-2000	Limited 2.5v	Limited 2.5v
Detector X1/25 Input (mv.)	0.1-80	80-400	400-2000	Limited 2.5v
Detector X1/125 Input (mv.)	0.02-16	16-80	80-400	400-2000
S1 Bit	0	1	0	1
S2 Bit	0	0	1	1
Open Linear Gate	X1	X1/5	X1/25	X1/125
Multiply Output Pulse Train By	1	5	25	125

PRINTED CIRCUIT BOARD

Figure 4 is the printed circuit card artwork for the 10^5 pulse height analyzer. This card has printed circuitry on both sides.

LINEAR GATE

Figure 5 is an electrical schematic diagram of the linear gate module. A detailed description of the linear gate is given in reference (b). The shaper section is deleted in this application since the detector pre-amplifiers shape the input

signal. The signal at the output of the linear gate when open, is twice that at the input to the 10^5 pulse height analyzer. Thus, the 2.5 millivolts to 2.0 volts range is converted to 5.0 millivolts to 4.0 volts at the output of the linear gate. The gain of transistor amplifier stages Q1-Q2 is adjusted by selection of R-8 to obtain this output.

SWEEP

Figure 6 is an electrical schematic diagram of the sweep module. A detailed description of the sweep circuit is given in reference (b). In this application, a tunnel diode (CR-12, Figure 6) has been included at output 2 to interface with the circuitry in the P.H.A. output gate. As indicated previously, the input linear range of signals to the sweep is 5.0 millivolts to 4.0 volts. The sweep output pulse width, effectively driving the P.H.A. output gate, is 2.0 microseconds per 5.0 millivolts of the input.

P.H.A. OUTPUT GATE

Figure 7 is an electrical schematic diagram of the P.H.A. output gate module. The function of this module is to:

a. initiate the 500 kHz output pulse train when there is an enable pulse coincident with a signal from the sweep,

b. generate an output to start the sweep capacitor discharge at the instant the 500 kHz output pulse train is initiated and

c. terminate the 500 kHz output pulse train at the instant the signal from the sweep returns to zero.

Transistor stages Q1 and Q2 convert the sweep output voltage swing of 0.0 volts to +0.5 volts into terminal 8 to the voltage swing of 0.0 volts to -0.24 across R5, as required by the following circuitry. With 0.0 volts at terminal 8, Q2 conducts and Q1 is cut off since Q2 base is at common while half the voltage at the collector of Q2 is fed back to the base of Q1. With Q1 not conducting, the voltage across R5 is zero. With +0.5 volts at terminal 8, Q1 is conducting and Q2 is cut off since the base of Q1 is at a more positive voltage than the base of Q2. The approximately 1.0 milliamperes of current flowing in the collector circuit of Q1 yields -0.24 across R5. The voltage across R5 is fed to the base of Q3. This is one input of the two input NAND gate consisting of transistor stages of Q3, Q4 and Q5. The enable input pulse feeds the base of Q4, which is the

second input to the NAND gate. The common emitters at Q3, Q4 and Q5 are driven by the constant current of 1.0 milliampere through R8. The common collectors of Q3 and Q4 are connected to R7 and the voltage developed across R7 is fed to the base of Q5. When either base of Q3 or Q4 is at zero volts, its collector to emitter circuit conducts and a voltage of -0.24 volts is developed across R7. This voltage fed to the base of Q5, cuts off Q5. When the voltage on both bases of Q3 and Q4 is -0.24 volts, these transistors are cut off with the voltage across R7 at zero volts. This zero voltage fed to the base of Q5, causes Q5 to conduct. Thus, when both a signal from the sweep (-0.24 volts on Q3 base) and the enable input (-0.24 volts on Q4 base) are present, the voltage across R7 is zero. The zero voltage across R7, fed to the base of Q6, sets the flip-flop consisting of transistor stages Q6, Q7, Q8 and Q9. This flip-flop consists of two cross coupled NAND gates with the set signal coming into the base of Q6 and the reset signal coming into the base of Q9. The outputs are taken across R9 and R10. The reset signal to the base of Q9 comes from the sweep output inverted signal across R5. Thus, the flip-flop is held in reset with no output from the sweep and is set when a signal is received from both the sweep and enable, and then reset when the sweep output returns to zero. The output from the flip-flop across R9 is fed to the base of Q15. This is one input of a two input NAND gate consisting of transistor stages Q13, Q14 and Q15. The second input comes from the free running 500 kHz square wave oscillator. The output of this NAND gate, across R25, is the square wave pulse train existing while the flip-flop is in the set stage. The output is fed through the level shifter, consisting of transistor stages Q10 and Q11, and drives output transistor Q12. The signal at the base of Q10 swings between zero znd -0.24 volts. At zero volts, Q10 conducts, yielding a voltage of -0.24 volts across R13. This voltage fed to the base of Q11, cuts off Q11. Q12 is turned on by the current flowing into its base to emitter circuit through R14. For -0.24 volts on the base of Q10, Q10 is cut off and Q11 conducts. The resultant -0.5 volts on the collector of Q11 and base of Q12, cuts off Q12. Thus, the pulse train output is obtained at terminal 10 with Q12 turning on and off at the pulse train frequency. This arrangement allows a wide range of resistors and voltages to be connected to pin 10 so that a wide variety of TTL, DTL, MOS or CMOS counters may be driven. The second output from the Q6, Q7, Q8 and Q9 flip-flop, across R10, drives the level shifter consisting of transistor stages Q16 - Q17. This is similar to the level shifter described previously. The output, from across R22, drives the Q18 - Q19 amplifier stage. The output from this stage through terminal 11 goes to the sweep to control the sweep capacitor discharge. With the flip-flop reset (no sweep output), a voltage of approximately -2.0 volts is obtained at terminal 11, holding off the sweep capacitor discharge. With the flip-flop set (sweep and enable signals), a voltage of approximately +2.0 volts is obtained at terminal 11, allowing the sweep capacitor to discharge.

THRESHOLD DETECTOR AND PULSER

Figure 8 is an electrical schematic diagram of the threshold detector and pulser module. This contains three separate threshold detector and pulse circuits. This circuitry is described in detail in reference (c). The threshold level of these detectors is approximately 220 millivolts.

FOUR RANGE DECISION CIRCUIT

Figure 9 is an electrical schematic diagram of the four range decision circuit module. As indicated previously, the function of this circuitry is to open the appropriate linear gate and indicate the multiplying factor to be applied when an event is processed. The logic required in performing this function is given in reference (a) and a logic diagram for this module is shown in Figure 3. Figure 9 shows that the logic required is obtained in this module by use of the NAND gate, bistables and level shifter circuits described previously for the P.H.A. output gate module. It will be noted that the basic gate circuit, in addition to yielding the NAND function, also yields the AND function (for example, across R8, R16, R25 and R32).

MODULE ARTWORK DRAWINGS

Table 2 lists the GSFC artwork drawing numbers from which the 10^5 pulse height analyzer cordwood welded modules were fabricated.

Table 2

Module Artwork Drawing Numbers

Unit	GSFC Drawing
Linear Gate	02-400B
Sweep	02-401B
P.H.A. Output Gate	02-430A
Threshold Detector and Pulser	02-422B
Four Range Decision Circuit	02-427B

CLOCK DRIVE CIRCUITRY

As indicated in Figure 3, the 10^5 pulse height analyzer requires inputs of:

a. 500 kHz oscillator square wave pulses,

b. the enable pulse and

c. the reset, write and transfer clock pulses.

These inputs are provided by the clock drive circuitry which is made up of discrete components and is assembled on a miniature terminal card. This card is mounted at the rear of the system board as shown in Figure 1.

Figure 10 is an electrical schematic diagram of the 500 kHz square wave oscillator and spiker circuitry mounted on the clock drive card. Transistor stage Q1 is a standard sine wave crystal oscillator. The sine wave output is fed to the base of Q2. Q2 and Q3 share a the common emitter resistor R7. Q3 base is connected to common. As the sine wave input to the base of Q2 crosses zero voltage in each direction Q3 conducts and is cut off alternately. This causes tunnel diode CR1 to switch between its high and low voltage states, yielding a square wave output. Resistor R8 is selected to set the d.c. bias on the base of Q2 to obtain a square wave at the output. This output is fed to the Q4 - Q5 pulse generator stage. This pulse generator, described in detail in reference (c), generates a spike at the junction of CR2 - CR-3 coincident with the trailing edge of the square wave.

Figure 11 is an electrical schematic diagram of the clock and buffer circuits mounted on the clock drive card. The function of these circuits is to:

a. generate the reset, write and transfer clock pulses in sequence upon receiving an input signal from the instrumentation logic system (indicating an event to be processed),

b. generate the output gate enable pulse and

c. buffer the 500 kHz square wave, enable pulse, reset, write and transfer clock pulse outputs to provide voltage and impedance match to the inputs in the four 10^5 pulse height analyzers.

When the instrumentation logic system determines that an event is to be processed (pulse height analyzed), a positive pulse is applied into terminal E5. The Q1 - Q2 buffer stage converts this positive input pulse to a negative pulse across R1

as required for operation of the following circuitry. The Q1-Q2 stage is similar to that for the P.H.A. output gate. The negative pulse across R1 drives both a spiker and a 5 microsecond delay pulse generator. The spiker, consisting of transistor stages Q3 and Q4, generates a normalized spike for each input pulse and drives the three series connected pulse generators Q5-Q6, Q7-Q8 and Q9-Q10. The spiker and pulse generator circuitry is described in detail in reference (c). These generate the reset, write and transfer clock pulses in sequence. The width of each of these pulses is adjusted by selection of L2, L3 and L4 to 200 nanoseconds. The reset, write and transfer pulse outputs from the generators go through their respective buffer circuits (Q11-Q12, Q13-Q14 and Q15-Q16) and on through terminals E7, E6 and E9 to the four 10^5 pulse height analyzers. The buffer circuits consist of a one input AND gate of the type described previously with low output impedances of 51 ohms so as to readily drive the four 10^5 pulse height analyzers.

The 5 microsecond delay pulse generator consists of transistor stages Q17 and Q18. This generates a 3 microsecond pulse delayed 5 microseconds after the event process input signal. This pulse generator is described in refereence (c). The delayed 3 microsecond pulse is fed into one input of the two input AND gate consisting of transistor stages Q19, Q20 and Q21. The spiker from the 500 kHz square wave oscillator, described previously, is fed into the second input of the AND gate. The output of this AND gate is generated across R47 and is the enable pulse. Thus, the enable pulse is generated at the trailing edge of the first 500 kHz square wave oscillator pulse occurring 5 microseconds after the event process pulse is obtained from the instrumentation system logic.

The arrangement described above assures that:

a. the sweep capacitor in the sweep circuit is fully charged to the peak of the input signal voltage before sweep discharge begins (because of the 5 microseconds delay),

b. the output pulse train always starts at the trailing edge of an oscillator pulse, thus eliminating jitter error in the output pulse train count, and

c. no spurious output pulse trains will be generated since the output pulse train may be initiated only during the 3 microsecond period following the event process input pulse with a sweep output signal present.

The enable pulse is fed through the buffer stage Q22-Q23 and out through terminal E8 to the four 10^5 pulse height analyzers. Buffer stage Q24-Q25

buffers the 500 kHz square wave oscillator through terminal E10 to the four 10^5 pulse height analyzers.

SYSTEM BOARD INTERCONNECTIONS

Figure 12 is an electrical interconnect diagram of the four 10^5 pulse height analyzer cards, the clock drive card and the input-output connectors.

POWER DRAIN

Table 3 lists the current and power drain of the assembled system.

(Table 3)

10^5 Pulse Height Analyzer System Current and Power Drain

Voltage	Current Drain (milliamperes)	Power Drain (milliwatts)
+12.0	0.6	7.2
+6.25	9.8	61.3
+2.25	39.0	87.8
-2.25	135.0	304.0
-6.25	15.8	98.8
-12.0	8.8	105.6
	Total	664.7

TEMPERATURE CHARACTERISTICS

The assembled system board operated satisfactorily in the temperature range -10°C to +40°C.

REFERENCES

a. Ciro A. Cancro, "Wide Range Pulse Height Analyzer With Data Compression Readout for Satellite Application," GSFC Report X-711-68-402, Nuclear Instruments and Methods, 73 (1969), pp. 61-66.

b. Ciro A. Cancro and Norman M. Garrahan, "Pulse Height Analyzer and Associated Threshold Detection and Logic Circuitry for General Satellite Application," GSFC Report X-711-68-274, Nuclear Instruments and Methods, Vol. 70:3 (1969) pp. 245-252.

c. Ciro A. Cancro, "Fast Low-Power-Drain Logic System for Use in Nuclear Experiments on Scientific Satellites," GSFC Report X-711-70-201, IEEE Transactions on Nuclear Science, October 1970, pp. 3-7.

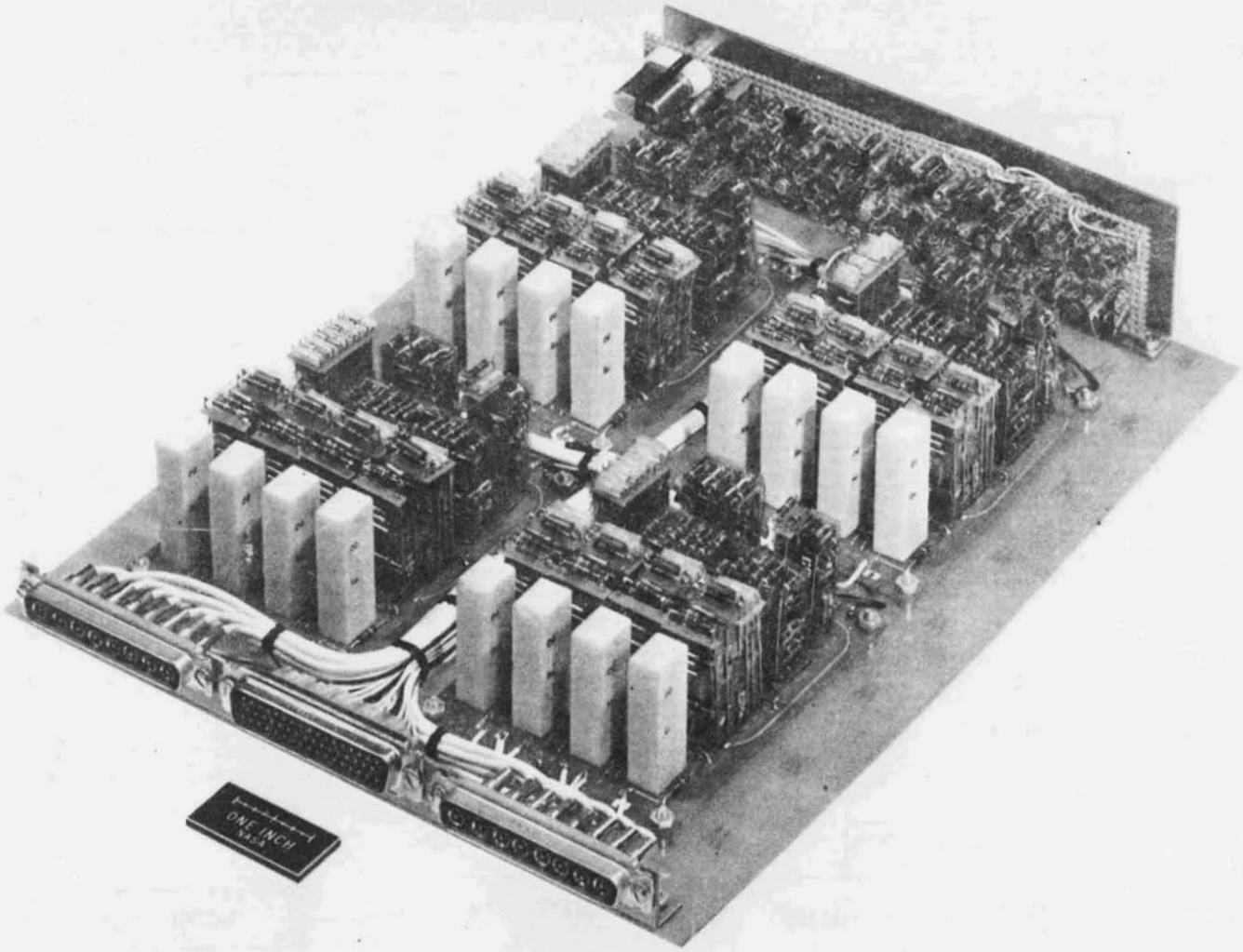


Figure 1. 10^5 Pulse Height Analyzer System Board

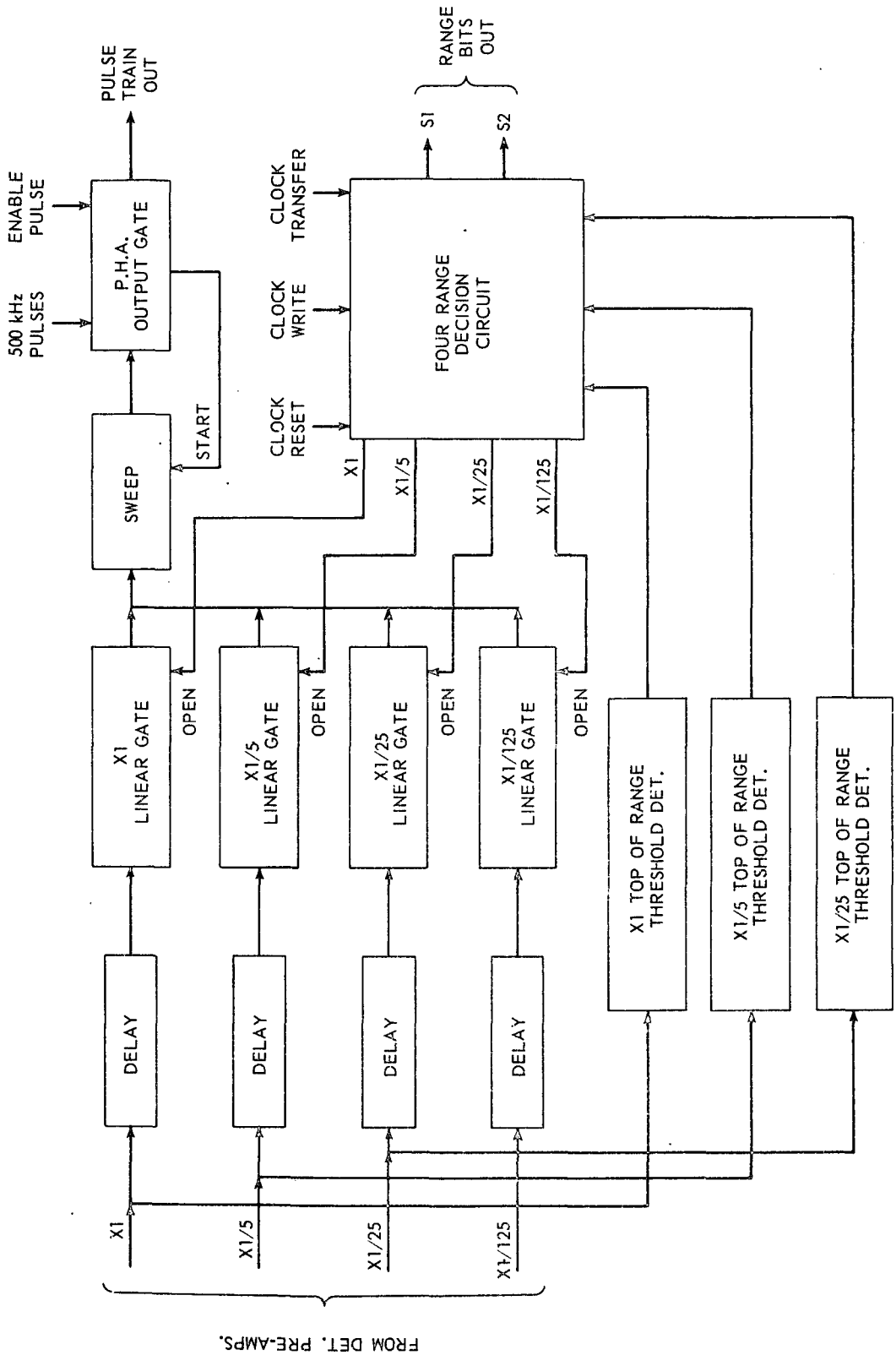


Figure 2. 10^5 Pulse Height Analyzer, Block Diagram

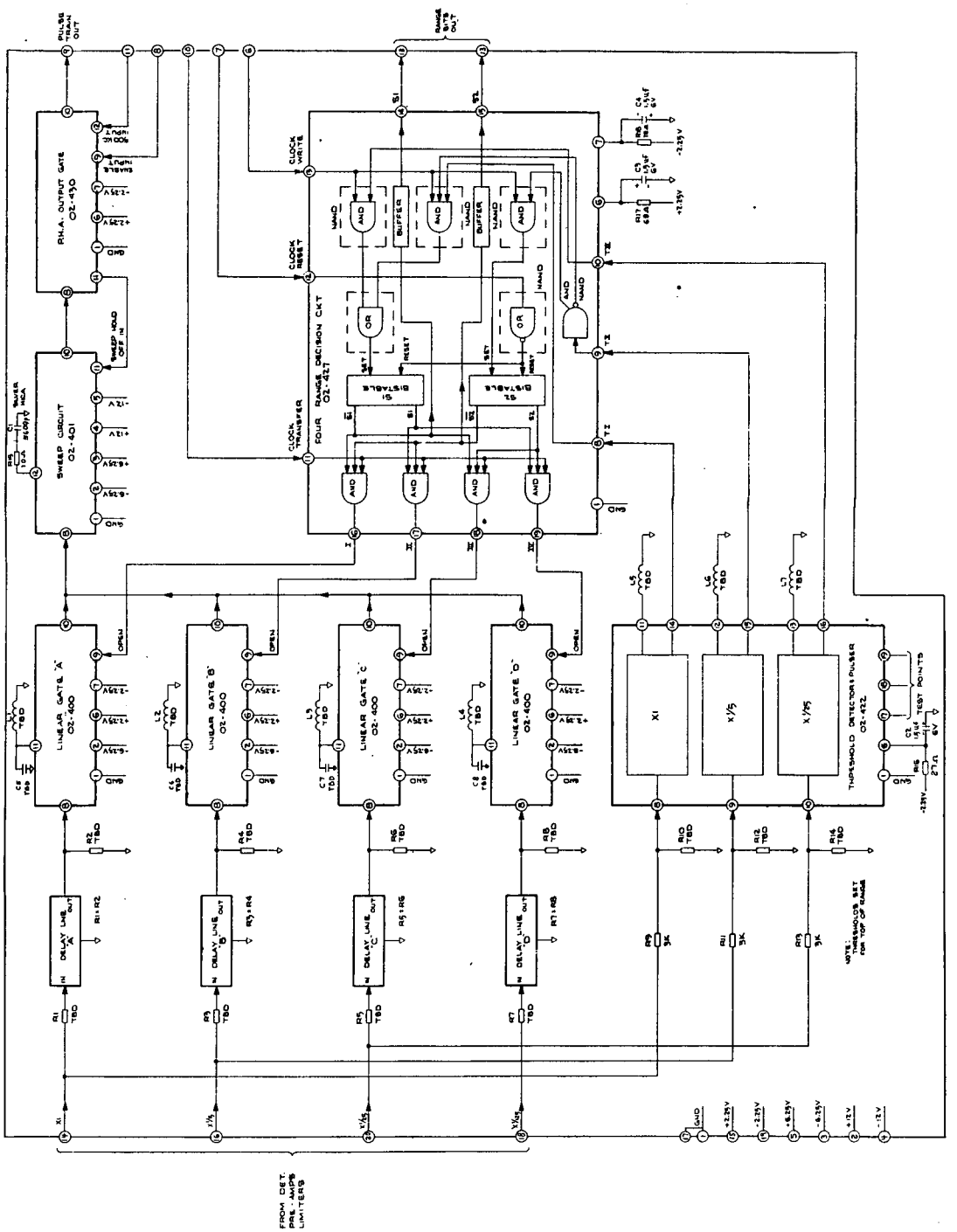


Figure 3. 10^5 Pulse Height Analyzer, Electrical Interconnect Diagram

DESIGNATION	DESCRIPTION
A1, A2, A3, A4	AIRTRONIC 266 DELAY LINE
4 REQD	02-400 LINEAR GATE
1 REQD	02-401 SWEEP CIRCUIT
1 REQD	02-426 THRESHOLD DET. & PULSER.
1 REQD	02-427 FOUR RANGE DESIGN CKT.
1 REQD	02-430 P.H.A. OUTPUT GATE.
R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R15	
R16, R17, R18	RESISTOR 1/8 W, 2.5% TBD
R9, R11, R13	RESISTOR 1/8 W, 2.5% 3K.
C2, C3, C4	CAPACITOR .1 C.A.F., 6V
C1	CAPACITOR (TBD) SILVER MICA
L5, L6, L7	CHOKE (TBD)
20 REQD	TERMINALS, CAMBION 208B-E MOUNT IN B HOLES

NOTES:

1. MATERIAL - .062 THK EPOXY GLASS LAMINATE TYPE GF, 10R. COPPER CLAD, BOTH SIDES, TYPE FL-GF-062-CU1 PER MIL-P-13949.
2. ETCH AND SOLD DIP PER SSEC-S-765-P-S.
3. ASSEMBLE PER SSEC-S-762-P-S.
4. SINGLE STRAIN RELIEF REQUIRED ON ALL HORIZONTALLY MOUNTED COMPONENTS.
5. ALL MODULES TO BE INSTALLED WITH PIN LAYOUT FILM ON BOTTOM OF MODULE.
6. "X" INDICATES B-BAR FEED THRUS
7. DRILL SIZES -
   - A — .093 DIA (#42)
   - B — .047 DIA (3/64)
   - C — .042 DIA (#55)

   ALL OTHER .028 DIA (#70)
8. ALL UNUSED MODULE LEADS TO EXTEND APPROX. 1/4" BEYOND BOARD AFTER MODULE INSTALLATION.

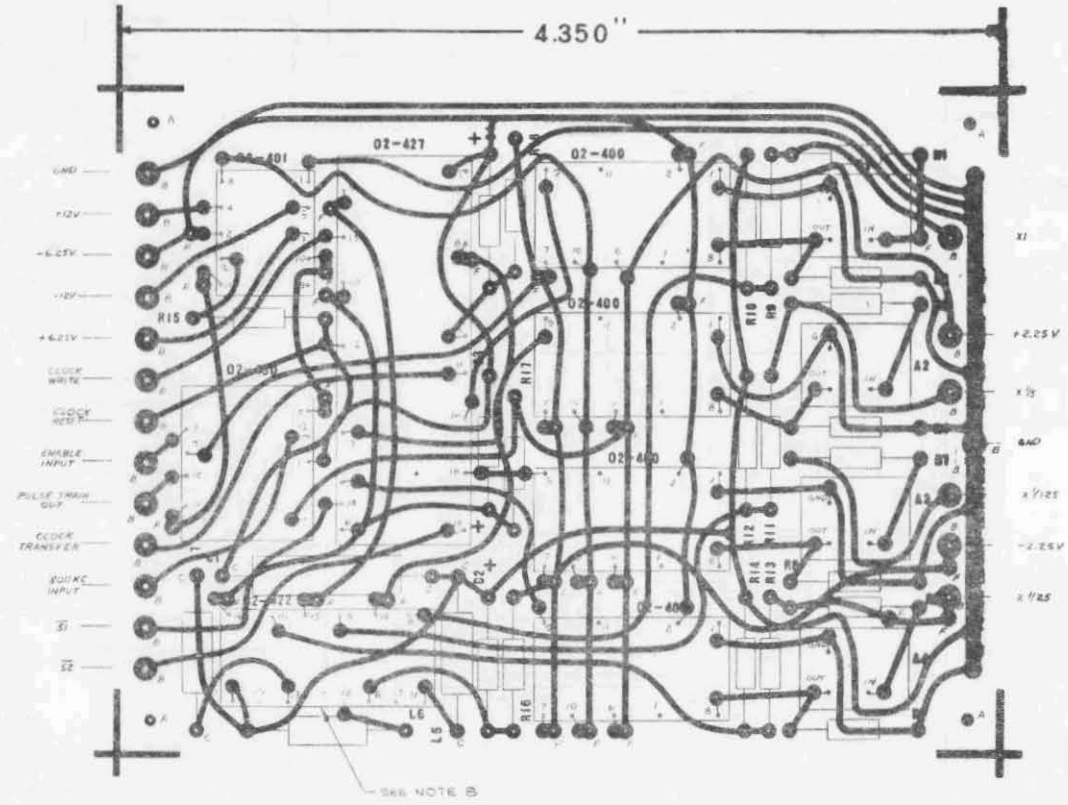


Figure 4. 10^5 Pulse Height Analyzer, Printed Circuit Card Artwork

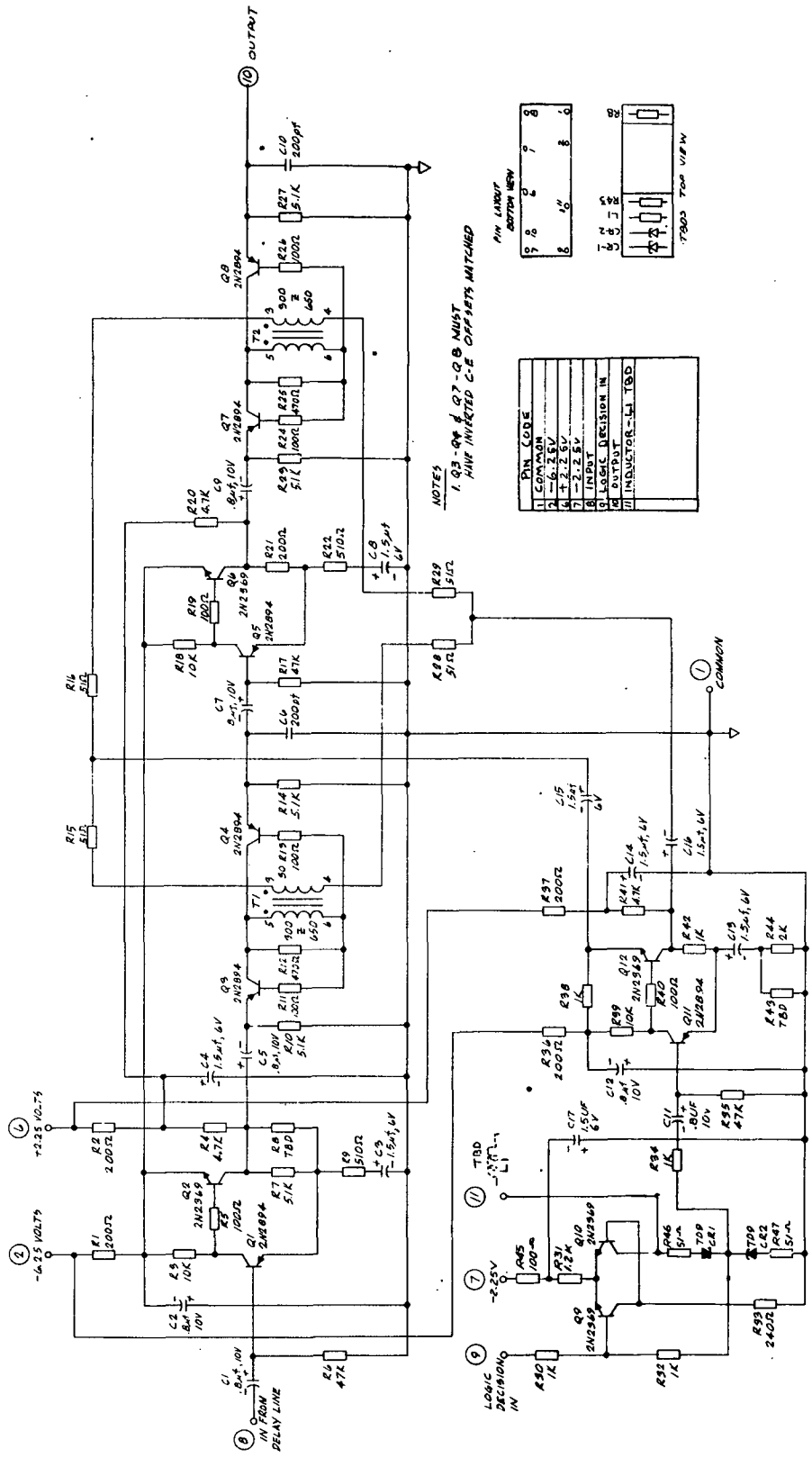


Figure 5. Linear Gate, Electrical Schematic Diagram

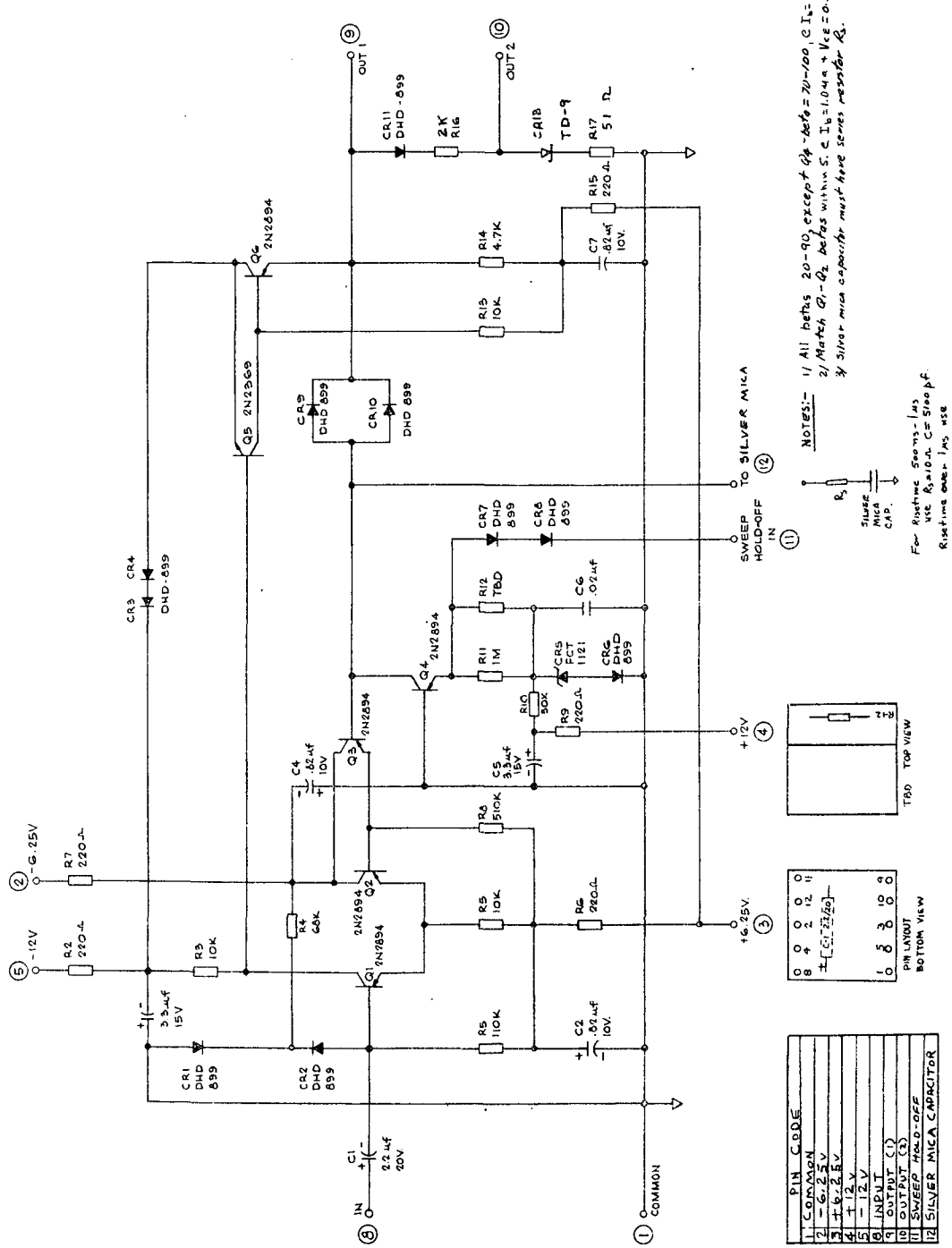


Figure 6. Sweep, Electrical Schematic Diagram

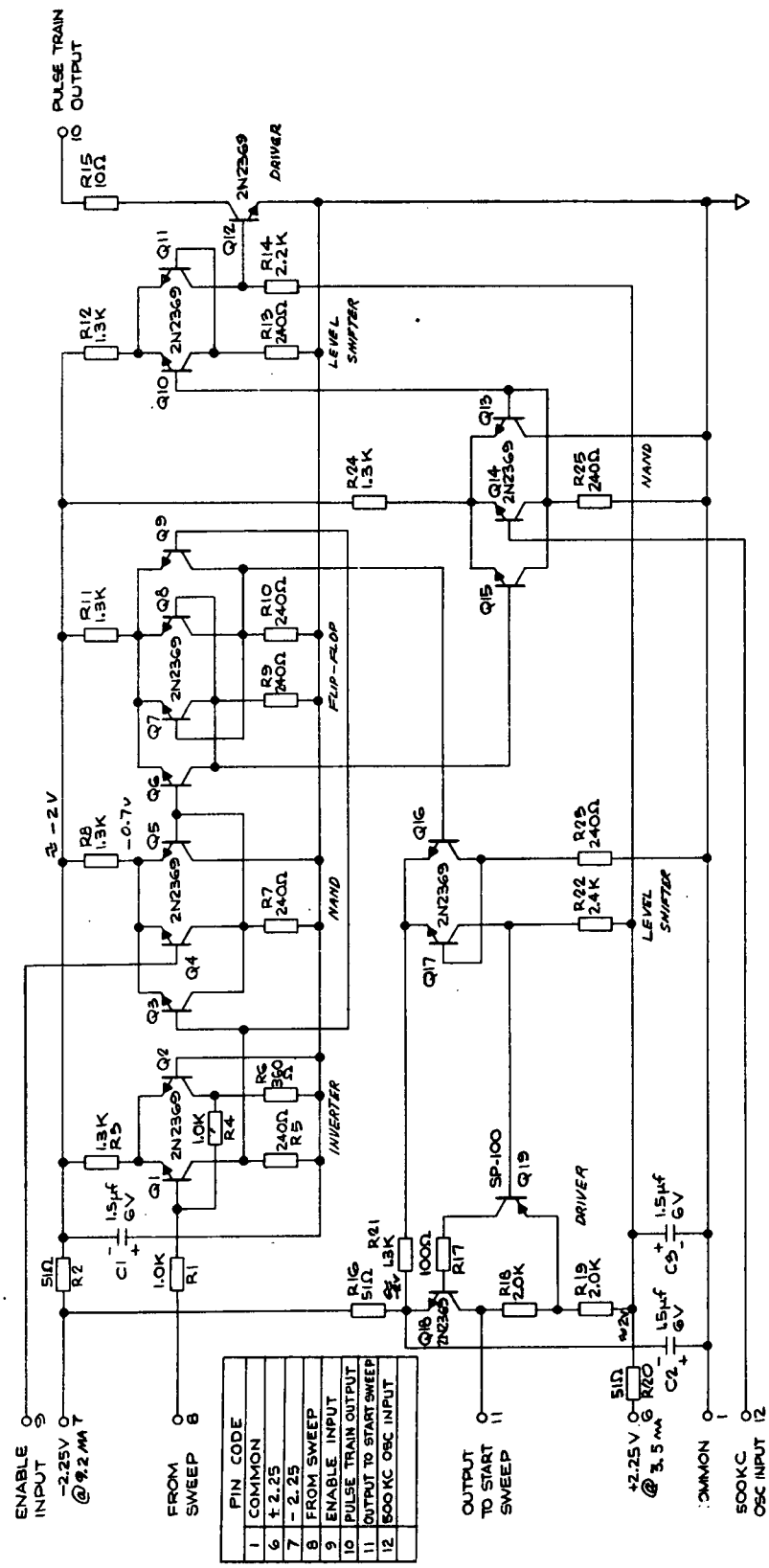
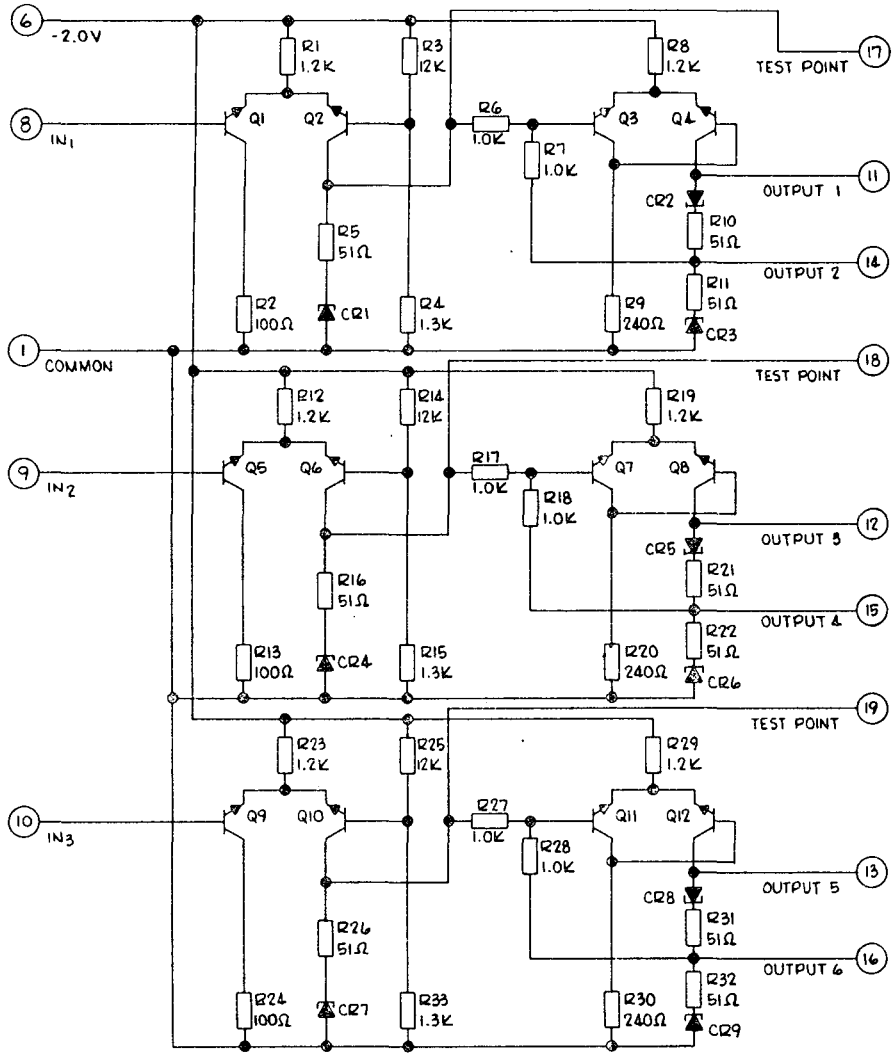


Figure 7. P.H.A. Output Gate, Electrical Schematic Diagram



NOTES:
UNLESS OTHERWISE NOTED
1. ALL RESISTORS ARE 1/4 W, ±5% CARBON
2. ALL TRANSISTORS ARE 2N2369.
3. ALL DIODES ARE TBD.

Figure 8. Threshold Detector and Pulser, Electrical Schematic Diagram

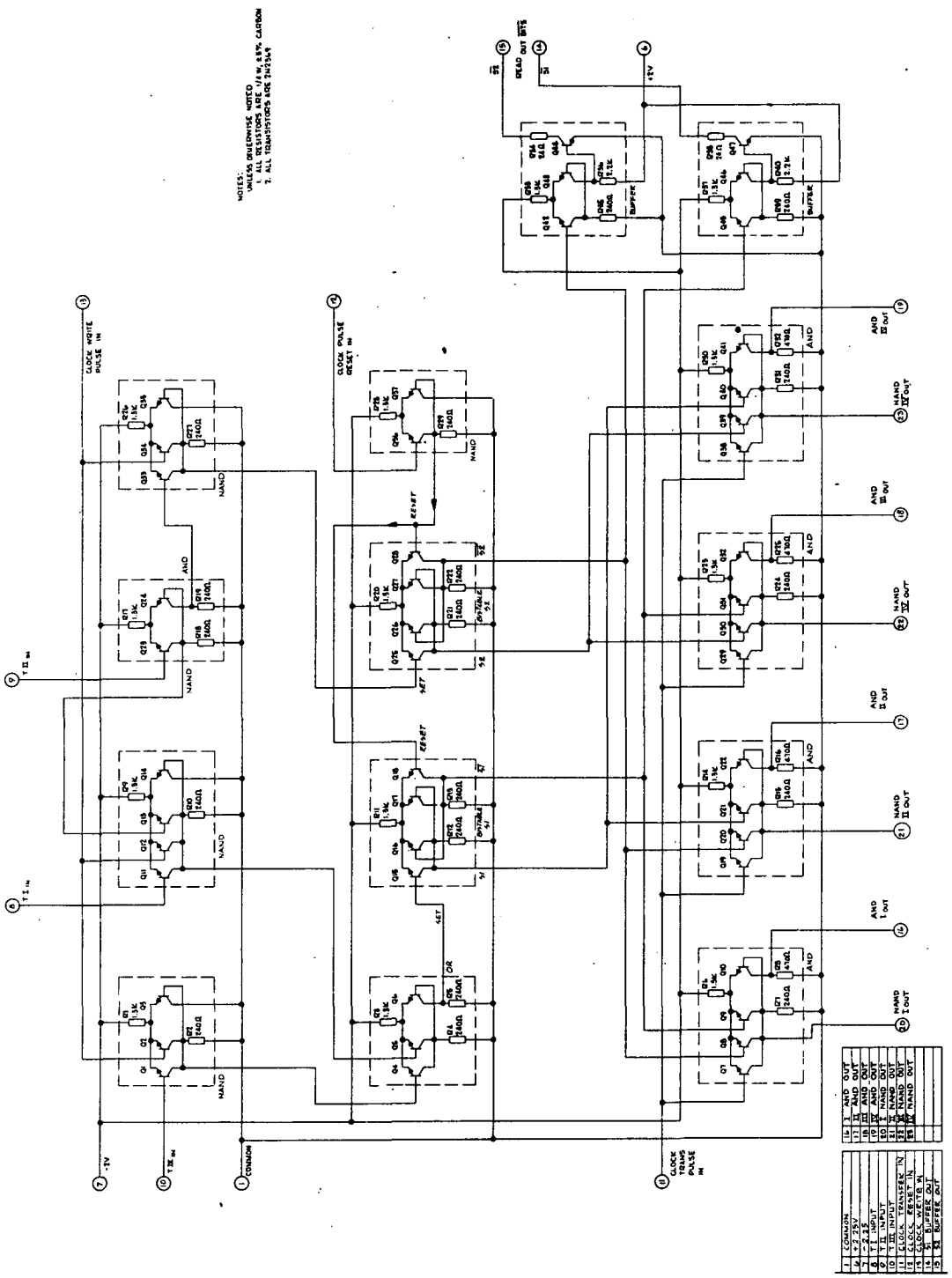


Figure 9. Four Range Decision Circuit, Electrical Schematic Diagram

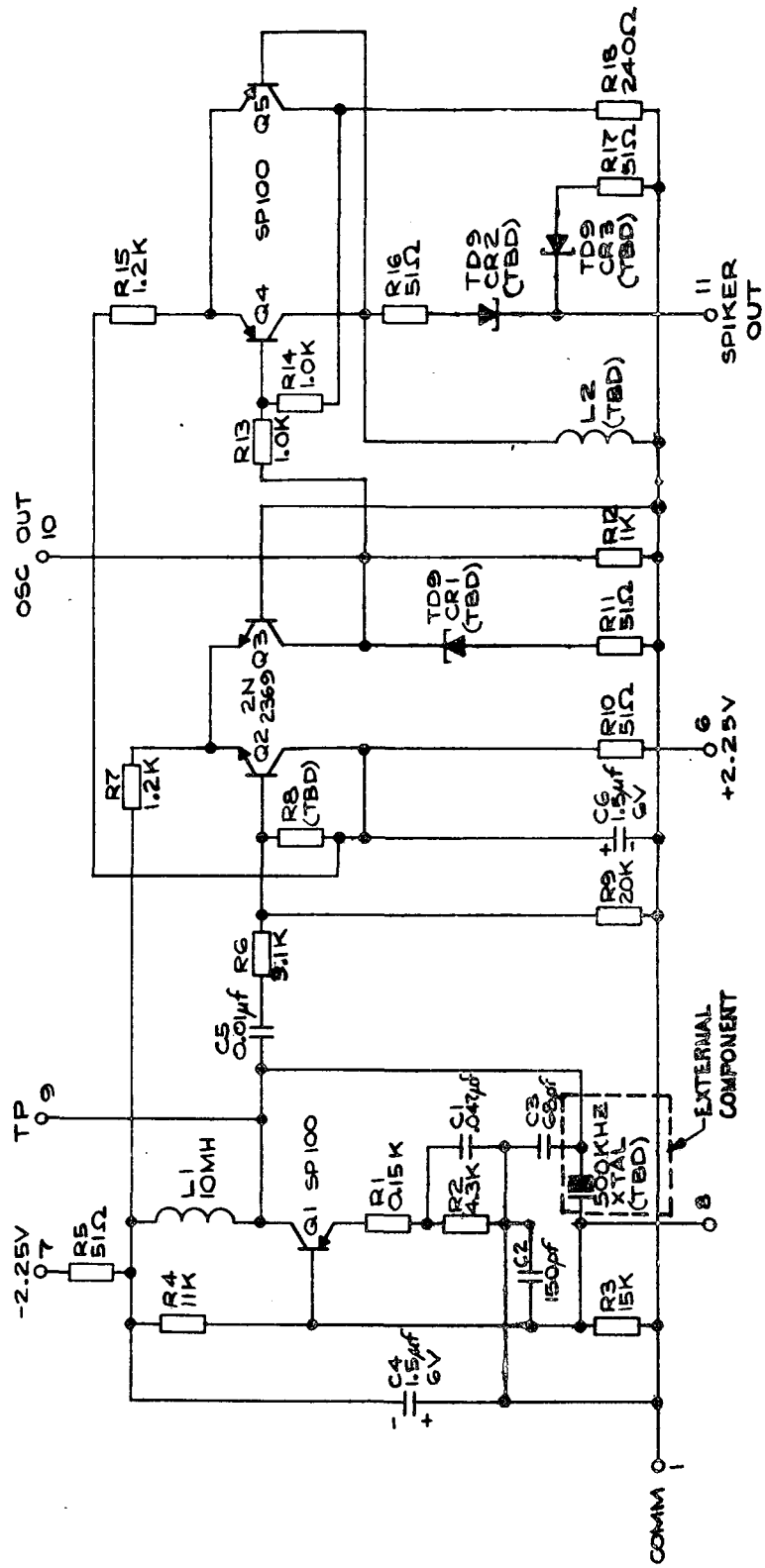


Figure 10. 500 kHz Square Wave Oscillator and Spiker, Electrical Schematic Diagram

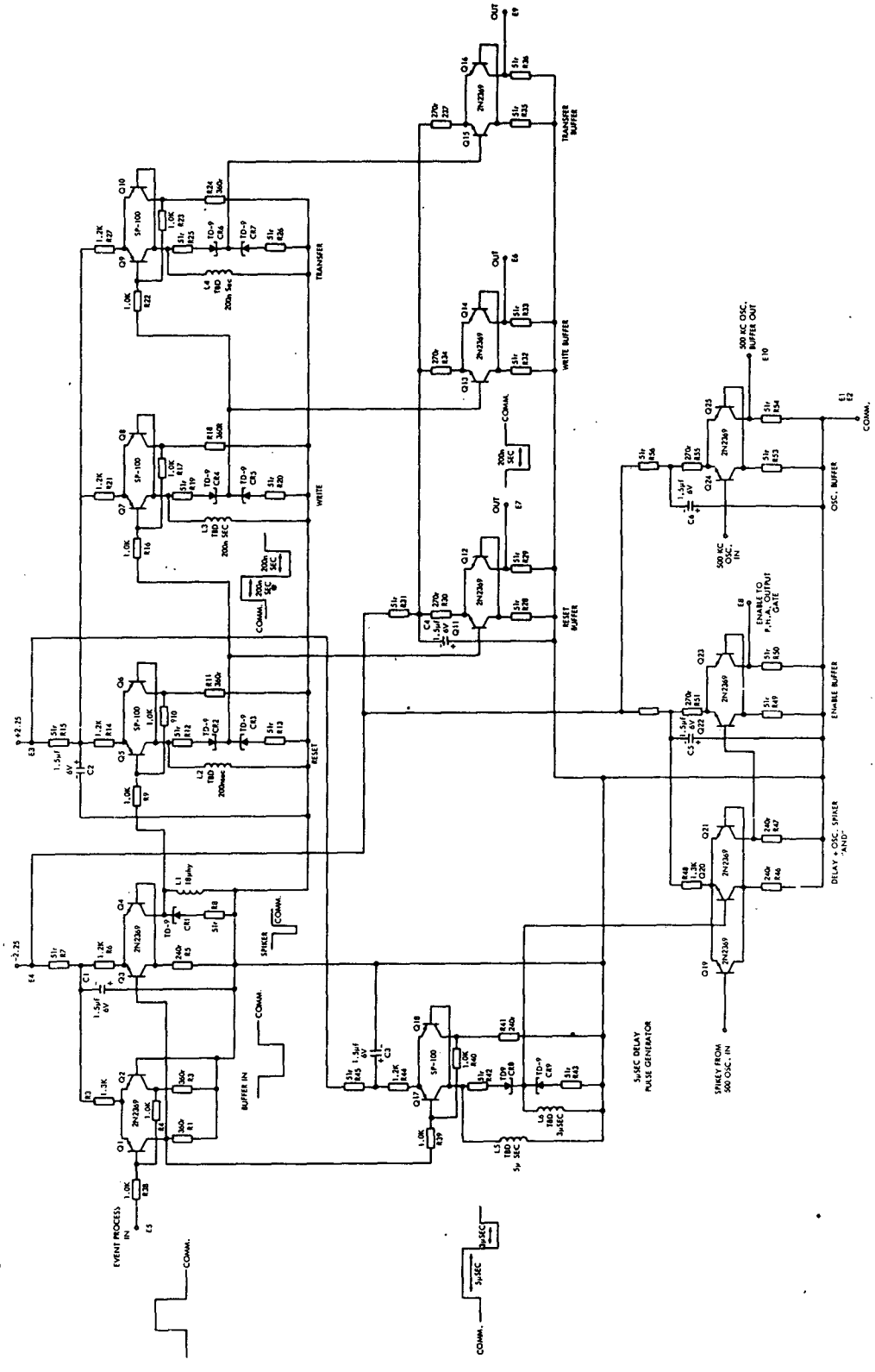


Figure 11. Clock and Buffer Circuits, Electrical Schematic Diagram

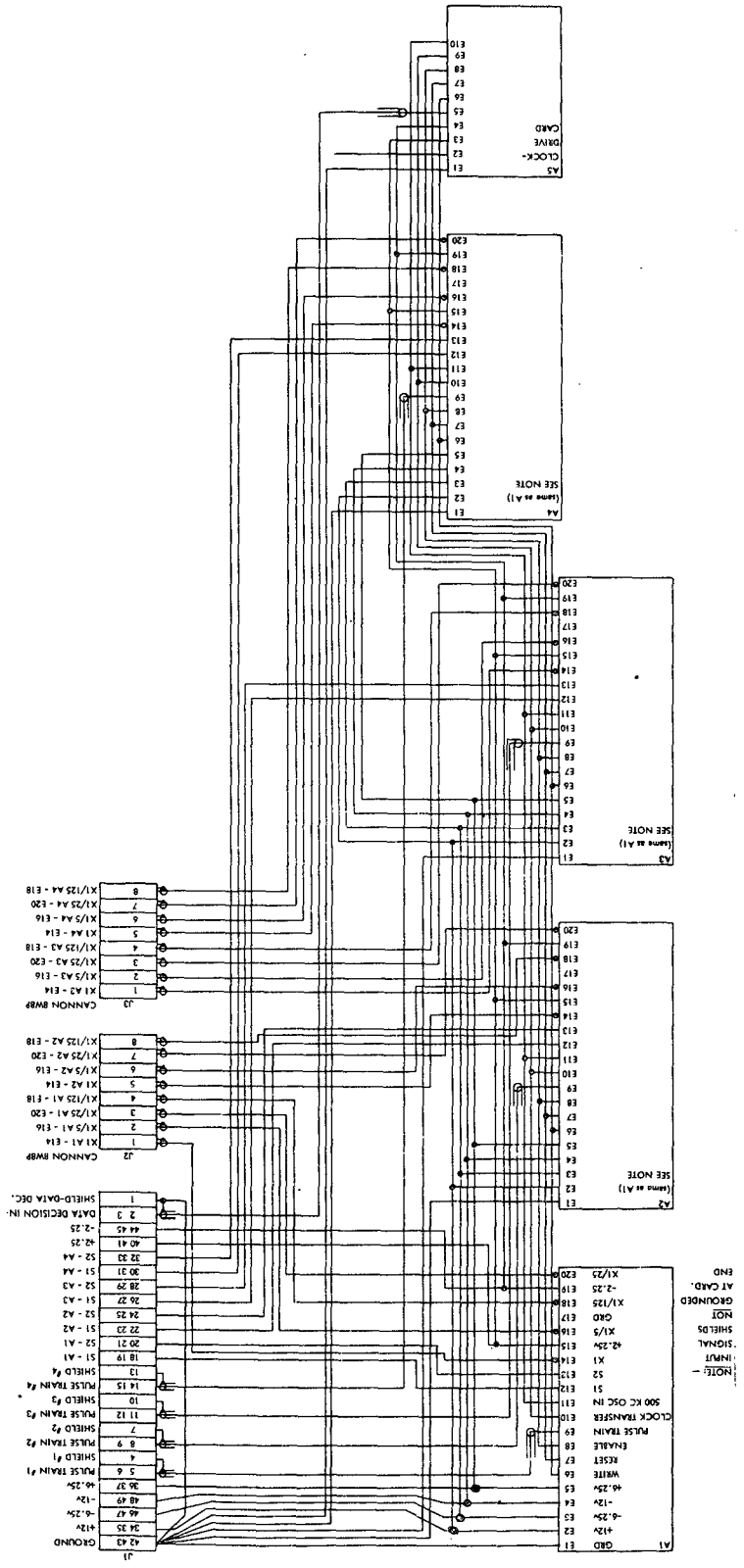


Figure 12. 10^5 Pulse Height Analyzer System Board Interconnections